Optimizing Image Signal Processing with RISC-V FPGA

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Introduction

ISPs (Image Signal Processors), similar to ISAs (Instruction Set Architectures), are typically proprietary and bound by licensing agreements, leading to vendor lock-in with non-standard, proprietary interfaces for sensors and ISPs. In this demonstration, Infinite ISP, a fully open-source soft IP, is coupled with a soft RISC-V SOC, creating a flexible and highly customizable platform that accelerates ISP development, eliminating licensing constraints, proprietary limitations, and vendor lock-in.

Hardware Specifications

The demonstration platform utilizes the Efinix® Sapphire RISC-V SoC based on VexRiscv core (a 32-bit CPU using ISA RISCV321 with M, A, F, D and C extensions)

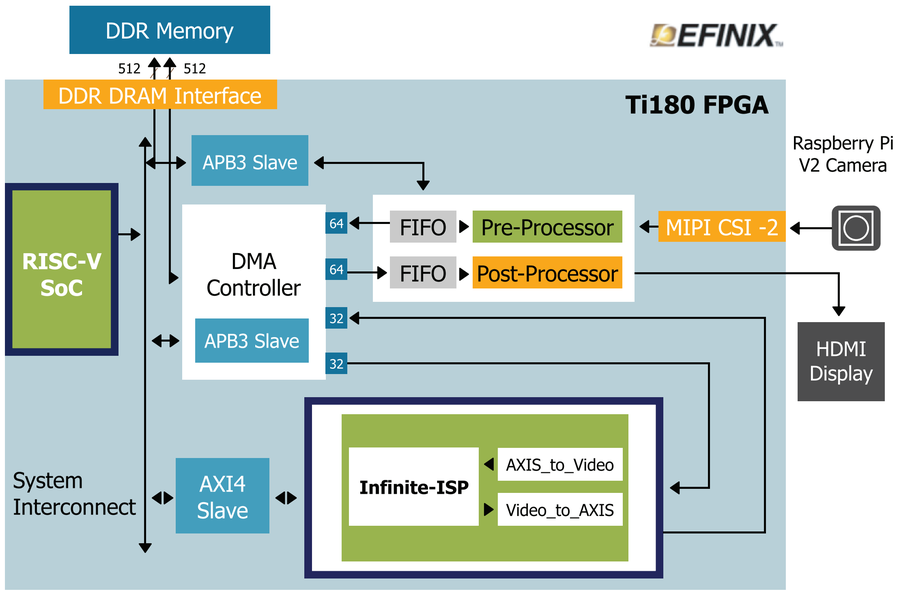
- User configurable Core
- AXI4 and APB3 bus support
- Core Freq: 300Mhz
  Peripheral Freq: 100Mhz
- UART, SPI & I2C
- No floating point Unit
- Instruction and Data Cache Size 4096Kb

The soft RISC-V SOC is coupled with Infinite ISP as the hardware acceleration block for edge vision applications.

- 10-bit ISP for Bayer Image Sensors
- Max Frame Size : 2048x1536
- Pixel Throughput: Up to 125MP/s
- 2A Statistics Engine: Adjustable AE, AWB
- Multi-level Noise Reductiion
- Selectable RBG, YUV444, YUV422 output

The entire system includes embedded compute and custom hardware all in the Efinix ® Titanium ® Ti180 J484 Development Kit

FPGA Demonstration Platform



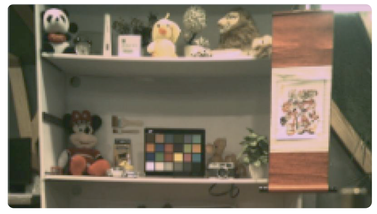
Resource Utilization

Block	XLR	LUT	FF	ADD	RAM	DSP
Complete Design (Implementation)	133,454 (77.2%)	-	-	-	379 (29.6%)	155 (31.8%)
Complete Design (Synthesis)	-	95,174	50,238	10,077	379	208
RISC-V SOC	-	11,014	15,908	795	105	4
DMA Controller	-	15,228	8,563	1,094	64	0
Other Logic	-	2,053	1,589	570	68	0
SD Host Controller	-	3,495	3,481	482	12	0
HW Accelerator Infinite-ISP	-	63,350	20,430	7,103	129	204
Infinite-ISP (only)	-	25,950	14,034	7,082	105	204

Key Challenges

- Interconversion between DMA AXI Stream and Infinite ISP DVP protocol
- 10-bit raw data packing for replacing RGB conversion
- 2A operation overload on RISC-V CPU

Objective Image Quality



Mean DeltaC =24.5

Efinix EVSoC Ti180 Reference Design

Mean DeltaC =9.8

Infinite-ISP Ti180 Reference Design

Design Optimization

Design	ISP Config	Fmax	LUT	FF	ADD	RAM	DSP	Tool
Zynq Ultrascale+	10-bit 2048x1536	125 MHz	43,531	22,482	-	42.5	58	Vivado
Titanium	10-bit 1952x1112	128 MHz	25,950	14,034	7,082	105	204	Efinity

Conclusion

Leveraging a RISC-V SOC core with the open-source Infinite ISP demonstrates high-quality output with a well-optimized, flexible design showcasing the potential of open hardware solutions in the word of computer vision